**Laboratory Report Cover Sheet**

**18ECE206J ADVANCED DIGITAL SYSTEMS DESIGN**

**Fourth Semester, 2021-22 (Even semester)**

SRM Institute of Science and Technology College of Engineering and Technology

Department of Electronics and Communication Engineering

**Name :**

**Register No. :**

**Day/ Session :**

**Venue :**

**Title of Experiment:**

**Date of Conduction:**

**Date of Submission :**

|  |  |  |
| --- | --- | --- |
| **Particulars** | **Max. Marks** | **Marks**  **Obtained** |
| Pre lab and Post lab | 10 |  |
| Lab Performance | 20 |  |
| Simulation and results | 10 |  |
| Total | 40 |  |

**REPORT VERIFICATION**

**Staff Name : Signature :**

**12. Design of sequential circuits 4-bit up counter**

**Aim:** To design and implement a sequential circuit 4-bit counter in VHDL.

**Software Required:**

Xilinx ise & ModelSim

#### Theory:

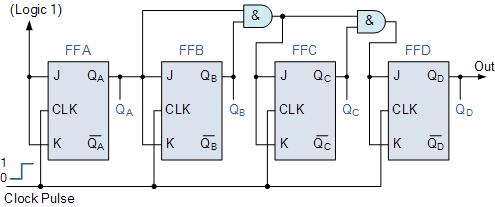
Circuits for counting events are frequently used in computers and other digital systems. Since a counter circuit must remember its past states, it has to possess memory. The number of flip flops used and how they are connected determine the number of states and the sequence of the states that the counter goes through in each complete cycle. Counters can be classified into two broad categories according to the way they are clocked:

* 1. Asynchronous (Ripple) Counters - the first flip-flop is clocked by the external clock pulse, and then each successive flip -flop is clocked by the Q or Q' output of the previous flip -flop.
  2. Synchronous Counters - all memory elements are simultaneously triggered by the same clock.

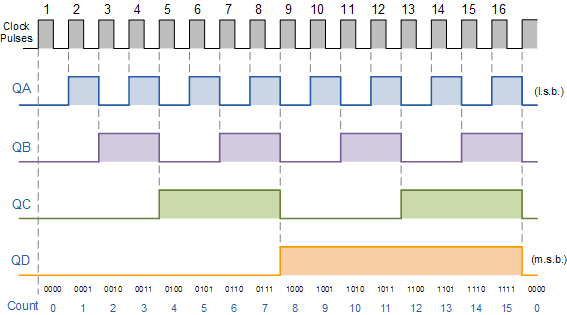
**Synchronous Counters:**

In *synchronous counters*, the clock inputs of all the flip-flops are connected together and are triggered by the input pulses. Thus, all the flip-flops change state simultaneously (in parallel). The circuit below is a 4-bit synchronous counter. It can be seen that, the external clock pulses (pulses to be counted) are fed directly to each of the J-K flip-flops in the counter chain and that both the J and K inputs are all tied together in toggle mode, but only in the first flip-flop, flip-flop FFA (LSB) are they connected HIGH, logic “1” allowing the flip-flop to toggle on every clock pulse. Then the synchronous counter follows a predetermined sequence of states in response to the common clock signal, advancing one state for each pulse. The J and K inputs of flip-flop FFB are connected directly to the output QA of flip-flop FFA, but the J and K inputs of flip-flops FFC and FFD are driven from separate AND gates which are also supplied with signals from the input and output of the previous stage. These additional AND gates generate the required logic for the JK inputs of the next stage. If we enable each JK flip-flop to toggle based on whether or not all preceding flip-flop outputs (Q) are “HIGH” we can obtain the same counting sequence as with the asynchronous circuit but without the ripple effect, since each flip-flop in this circuit will be clocked at exactly the same time.

Then as there is no inherent propagation delay in synchronous counters, because all the counter stages are triggered in parallel at the same time, the maximum operating frequency of this type of frequency counter is much higher than that for a similar asynchronous counter circuit.



**Fig 1: Binary 4-bit Synchronous up Counter**



**Fig. 2 4-bit Synchronous Counter Waveform Timing Diagram.**

**VHDL Code for** **Binary 4-bit Synchronous up Counter:**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity UPCOUNTER is

Port ( CLK,RST : in STD\_LOGIC;

COUNT : inout STD\_LOGIC\_VECTOR (3 downto 0));

end UPCOUNTER;

architecture Behavioral of UPCOUNTER is

begin

process (CLK,RST)

begin

if (RST = '1')then

COUNT <= "0000";

elsif(rising\_edge(CLK))then

COUNT <= COUNT+1;

end if;

end process;

end Behavioral;

**Pre-lab questions**

1. How does synchronous counter differ from asynchronous counter?
2. What is the difference between the latch, flip-flop and master –slave Flip-flop?
3. Give the Transition table and excitation table of JK Flip flop.
4. A 4-bit up/down binary counter is in the DOWN mode and in the 1010 state. On the

next clock pulse, to what state does the counter go?

**Post-lab questions**

1. Deign a 3-bit Up/Down Gray Code Counter using D Flip-flop
2. Convert D Flip-flop to JK Flip-flop
3. What are the advantages of an edge-triggered Flip-flop over a level-triggered device?
4. A 4-bit binary synchronous counter uses Flip-flops with propagation delay time of 25ns each. The maximum possible time required for change state will be --------------.

**Result**